3DRC3508ES2861

PRODUCT OVERVIEW

The 3DRC3508ES2861 is an octal 3-input high-speed Majority Voter with integrated redundancy. Operating across a voltage supply range of 1.65 V to 5.5 V, it offers four dual 3-input voter gates, with individual error outputs.

Dedicated « error detected » indication are available (EDET_*ij*), in addition to external error input signals (EIN_*ij*). Cold sparing is supported allowing any redundant configuration, along with ESD protection on all inputs and outputs.

Featuring specific radiation effect mitigation techniques and utilizing space design de-rating rules, the Rad Hard by Design 3DRC3508ES2861 Majority Voter is an ITAR free product and features a SEL/SET LET_{th} of 74.7 MeV.cm^2/mg and a TID of 30 krad(Si).

The 3DRC3508ES2861 is manufactured with 3D PLUS space qualified stacking technology designed for high reliability applications and is available in a compact size and low weight SOP package.

KEY FEATURES

- 1.65 V to 5.5 V voltage range
- Input voltage up to 5.5 V at any V_{cc}
- Provides logic-level down translation to V_{cc}
- Cold sparing capability
- Internal power-on reset (POR) circuitry
- Power savings & low dissipated power
- 13 ns maximum propagation delay on data at 3.3 V
- Radiation Hardened design
  - TID > 30 krad(Si)
  - SEL and SET LET_{th} > 74.7 MeV.cm^2/mg
- Operating temperature –55°C / +125°C

LOGIC FUNCTION DIAGRAM

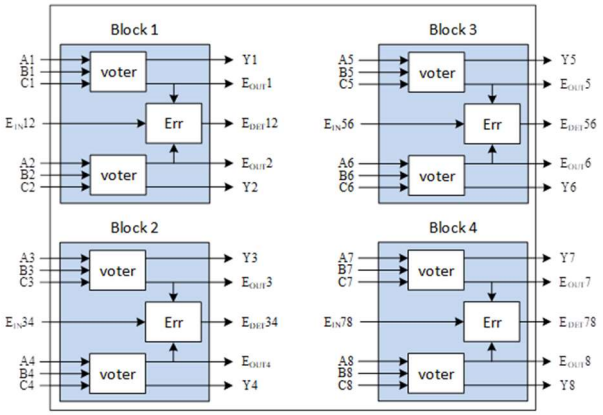

Figure 1 Block Diagram

PACKAGE

SOP 54 - Pitch 0.5 mm

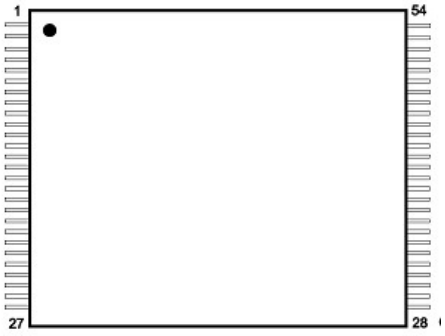

Figure 2 Package

TABLE OF CONTENT

FIGURES

TABLES

1. DOCUMENTS

1.1 APPLICABLE DOCUMENTS

The following documents, at the relevant issue in effect on the date of the purchase order placement, form a part of this specification to the extent specified herein, and shall be read in conjunction with it:

[AD1] PID 3D PLUS – ref. 3300-0546
[AD2] General requirements for EEE components procurement and incoming inspection – Ref. 3DPA-0350
[AD3] DETAIL SPECIFICATION - Octal 3-input Majority Voter 3DRC3508ES2861- ref. 3DPA-8331

1.2 REFERENCE DOCUMENTS

The following documents, at the relevant issue in effect on the date of the purchase order placement, form a part of this specification to the extent specified herein, and shall be read in conjunction with it:

[RD1] MIL-STD-883: “Tests Methods and Procedures for Microelectronics”
[RD2] MIL-PRF-38534: “Hybrid Microcircuits, General Specifications for”
[RD3] ECSS-Q-ST-60-05C: “Space Product Assurance – Generic procurement Requirements for Hybrid Microcircuits”.

2. ACRONYMS

ESD:	Electrostatic Discharge
CDM:	Charged Device Model
DPA:	Destructive Physical Analysis
GND:	GROUND
HBM:	Human-body model
LAT:	Lot Acceptance Test
Mbps:	Mega-bits per second
P/N:	Part Number
SEL:	Single Event Latchup
SEU:	Single Event Upset
SN:	Serial Number
SOP:	Small Outline Package
TBC:	To Be Confirmed
TID:	Total Ionizing Dose
TMR:	Triple Modular Redundancy

3. GENERAL DESCRIPTION

The 3DRC3508ES2861 is a 3-input, high-speed octal majority voter module with built-in triple redundancy. With the three 8-bit inputs used for majority voting, the module provides the result of the vote as an output, along with an error signal indicating if there is a difference between any of the input bits (also 8-bit).

Operating across a voltage supply range of 1.65 V to 5.5 V, it offers dedicated « error detected » indications, in addition to external error input signals. Cold sparing is supported allowing any redundant configuration, along with ESD protection on all inputs and outputs.

The 3DRC3508ES2861 is immune to SET and SEL by design, and insensitive to SEU/MBU by process (CMOS IC). Therefore, this radiation hardened by Design device is used in multiple space applications when Designers need to enhance the reliability of their systems by using TMR (Triple Modular Redundancy) technics.

The triple modular redundancy (TMR) is a fault-tolerant form of N-modular redundancy, in which three systems perform a process and that result is processed by a majority-voting system to produce a single output. If any one of the three systems fails, the other two systems can correct and mask the fault (see Table 1: Truth table).

3.1 TRUTH TABLE

INPUT			OUTPUT	
An	Bn	Cn	Yn	$E_{OUT}n$
L	L	L	L	L
L	L	H	L	H
L	H	L	L	H
L	H	H	H	H
H	L	L	L	H
H	L	H	H	H
H	H	L	H	H
H	H	H	H	L

INPUT	INTERNAL VOTING		OUTPUT
E_{IN}	$E_{OUT}1$	$E_{OUT}2$	E_{DET}
L	L	L	L
X	X	H	H
X	H	X	H
H	X	X	H

Table 1: Truth table

3.2 TYPE VARIANTS

VARIANT – PART NUMBER (Note 1)	Operating Temperature Range	Grade	Active Component LAT Option (Note 2)	Case (Figure 1 of AD3)	Leads Material and Finish
3DRC3508ES2861 IB	-40°C to +85°C	Industrial	Standard	SOP 54 pins – package CK2	Kovar Ni+Au plating
3DRC3508ES2861 IS	-40°C to +85°C	Space	Standard	SOP 54 pins – package CK2	Kovar Ni+Au plating
3DRC3508ES2861 IS1	-40°C to +85°C	Space	Extended	SOP 54 pins – package CK2	Kovar Ni+Au plating
3DRC3508ES2861 MS	-55°C to +125°C	Space	Standard	SOP 54 pins – package CK2	Kovar Ni+Au plating
3DRC3508ES2861 MS1	-55°C to +125°C	Space	Extended	SOP 54 pins – package CK2	Kovar Ni+Au plating

Table 2: Module Type Variants

Notes:

1. These variants are suitable for automatic and manual assembly process approved by ESA (PID 3300-0546).
   Module assembly on board must follow reflow guidelines as defined in: http://www.3d-plus.com/technical-documentation.php
2. Active component Lot Acceptance Test options are described in Annex 1. Standard LAT is derived from ECSS-Q-ST-60-05C, and Extended LAT is derived from ECSS-Q-ST-60-13C.

4. RADIATION PERFORMANCES

Parameters	Description	
TID	V_{CC} = 5.5 V	> 30 krad (Si)
SEL LET_{th}	V_{CC} = 5.5 V	> 74.7 MeV.cm²/mg
SET LET_{th}	V_{CC} = 5.5 V	> 74.7 MeV.cm²/mg

Table 3: Radiation performances

Note: The module embeds combinatorial logic ICs in CMOS process as active components, thus it is not subject to SEU and SEFI.

5. PIN ASSIGNMENT

Pin Nbr	Signal Name	Pin Nbr	Signal Name	Pin Nbr	Signal Name	Pin Nbr	Signal Name
1	V_{CC}	15	V_{CC}	28	GND	42	GND
2	EDET_12	16	EDET_56	29	EIN_78	43	EIN_34
3	EDET_34	17	EDET_78	30	EIN_56	44	EIN_12
4	EOUT2	18	EOUT6	31	EOUT7	45	EOUT3
5	EOUT4	19	EOUT8	32	EOUT5	46	EOUT1
6	Y2	20	Y6	33	Y7	47	Y3
7	Y4	21	Y8	34	Y5	48	Y1
8	C2	22	C6	35	C7	49	C3
9	C4	23	C8	36	C5	50	C1
10	B2	24	B6	37	B7	51	B3
11	B4	25	B8	38	B5	52	B1
12	A2	26	A6	39	A7	53	A3
13	A4	27	A8	40	A5	54	A1
14	GND			41	V_{CC}		

Table 4: Pin assignment

6. PIN DESCRIPTION

Signal Name	description
A[]	Logic inputs
B[]	Logic inputs
C[]	Logic inputs
Y[]	Logic outputs
E_{IN}[]	external voter **E**rror **IN**puts
E_{OUT}[]	external voter **E**rror **OUT**puts
E_{DET}_[][]	**E**rror **DET**ected outputs
V_{CC}	Positive Voltage supply
GND	ground

Table 5: PIN description

7. ELECTRICAL CHARACTERISTICS

The characteristics are given following the JEDEC standards, negative values representing current sourced from the device and positive values representing current sunk into the device.

7.1 ABSOLUTE MAXIMUM RATINGS

N°	CHARACTERISTICS	SYMBOL	MAX RATINGS	UNIT	REMARKS
1	Supply Voltage range	V_{CC}	-0.5 to +5.5	V	
2	Input Voltage range	V_I	-0.5 to +5.5	V	
3	Output Voltage range	V_O	-0.5 to V_{CC} + 0.5	V	Note 3
4	Maximum supply current	I_{CC}	400	mA	Note 2
5	Continuous output current (per pin & per block)	I_O	100	mA	
7	Storage Temperature Range	T_{STG}	-65 to +150	°C	
8	Maximum Junction Temperature	T_{JMAX}	+150	°C	
9	Body Temperature (short exposure only)	T_{BODY}	+235	°C	Measured at module side level (exposure < 60s)

Table 6: Absolute Maximum ratings

Note 1:
Permanent module damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating condition. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.
Note 2:
V_O must remain below absolute maximum rating of V_{CC}.
Note 3:
The overall maximum output current per module is 400 mA.

7.2 RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	MAX	UNIT
Supply Voltage range	V_{CC}	-	1.65	5.5	V
Input Voltage range	V_I	-	0	5.5	V
Output Voltage range (Note 1)	V_O	-	0	V_{CC}	V
Maximum bitrate per output (Note 2)		-	-	100	Mbps
High-level Input Voltage	V_{IH}	V_{CC} = 1.65 to 1.95 V	1.4	-	V
		V_{CC} = 2.3 to 2.7 V	1.9		
		V_{CC} = 3.0 to 3.6 V	2.5		
		V_{CC} = 4.5 to 5.5 V	3.8		
Low-level Input Voltage	V_{IL}	V_{CC} = 1.65 to 1.95 V	-	0.4	V
		V_{CC} = 2.3 to 2.7 V		0.6	
		V_{CC} = 3.0 to 3.6 V		0.9	
		V_{CC} = 4.5 to 5.5 V		1.35	
Input rise or fall time (10% - 90%)	t_r, t_f	V_{CC} = 1.65 to 1.95 V	-	1000	ns
		V_{CC} = 2.3 to 2.7 V		600	
		V_{CC} = 3.0 to 3.6 V		500	
		V_{CC} = 4.5 to 5.5 V		400	
Operating Junction temperature	T_j	-	-55	125	°C
Thermal resistance with underfill Junction-to-case (Note 3)	$Rth_{(J-C)}$	-	-	10	°C/W
Thermal resistance Junction-to-ambient (Note 4)	$Rth_{(J-A)}$	-	-	90	°C/W
Thermal resistance with underfill Junction-to-ambient (Note 5)	$Rth_{(J-A)\ underfill}$	-	-	50	°C/W

Table 7: Recommended operating conditions

Notes:

1. V_O must remain below absolute maximum rating of V_{CC}.
2. At module level this gives a maximum bitrate of 800 Mbps.
3. Case is defined as the temperature at the module lateral sides, Junction is defined as the highest Junction Temperature in the stack.
4. Ambient is defined as the temperature at the bottom of the leads in contact with the board.
5. In $Rth_{(J-A)\_underfill}$ (Thermal resistance Junction to Ambient with underfill), Ambient is defined as the temperature at the bottom of the leads in contact with the board. This module could be underfilled to ensure its performances at the temperature ranges specified in Table 2 . The underfill shall have a thermal resistance lower or equal to 5°C/W. We suggest to use an underfill with an area of 100 mm², a thickness of 1.4 mm and a thermal conductivity equal to 1.6 W/(m.K) (LOCTITE STYCAST 2850 MT CAT 27-1 for example) to achieve thermal performances.

7.3 STATIC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	I_O	V_{CC}	MIN	MAX	UNIT
Low-level Output Voltage	V_{OL}	100µA	1.65 V to 5.5 V	-	0.10	V
		1 mA	1.65 V to 5.5 V	-	0.25	
		4 mA	2.3 V	-	0.6	
			3.0 V	-	0.4	
			4.5 V	-	0.4	
		8 mA	2.3 V	-	1	
			3.0 V	-	0.8	
			4.5 V	-	0.6	
		16 mA	3.0 V	-	1.4	
			4.5 V	-	1.2	
		24 mA	4.5 V	-	1.5	
High-level output Voltage	V_{OH}	-100µA	1.65 V to 5.5 V	V_{CC} – 0.1	-	V
		-1 mA	1.65 V to 5.5 V	V_{CC} – 0.25	-	
		-4 mA	2.3 V	1.8	-	
			3.0 V	2.6	-	
			4.5 V	4.2	-	
		-8 mA	2.3 V	1.4	-	
			3.0 V	2.2	-	
			4.5 V	3.9	-	
		-16 mA	3.0 V	1.5	-	
			4.5 V	3.3	-	
		-24 mA	4.5 V	3.0	-	
High-level output current	I_{OH}		1.65 to 1.95 V	-	-4	mA
			2.3 to 2.7 V		-8	
			3.0 to 3.6 V		-16	
			4.5 to 5.5 V		-24	
Low-level output current	I_{OL}		1.65 to 1.95 V	-	4	mA
			2.3 to 2.7 V		8	
			3.0 to 3.6 V		16	
			4.5 to 5.5 V		24	
High-level input current	I_{LIL}		1.65 to 5.5 V	-1	+1	µA
Low-level intput current	I_{LIH}		1.65 to 5.5 V	-1	+1	µA
Standby supply current	I_{SB}	0 mA	1.65 to 5.5 V		820	µA
Power down leakage current (1)	I_{OFF}		OFF (2)		5	µA

Table 8: Static characteristics

Notes:

1. Into any input or output port.
2. V_{CC} is disconnected or at GND potential.

7.4 DYNAMIC CHARACTERISTICS

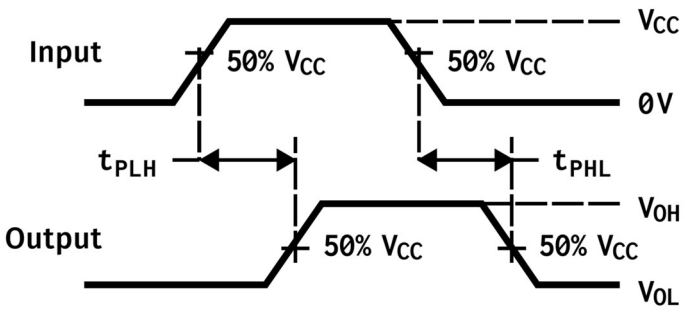

Figure 3 Propagation Delay measurement

CHARACTERISTICS	SYMBOL	CONDITIONS	V_{CC}	TYP	MAX	UNIT
Propagation Delay (A_n, B_n or C_n to output Y_n)	t_{pd}	C_L = 50 pF	4.5 to 5.5 V		11	ns
			3.0 to 3.6 V		13	
			2.3 to 2.7 V		15	
			1.65 to 1.95 V		25	
Propagation Delay (A_n, B_n or C_n to output E_{outn})	t_{err_det}	C_L = 50 pF	4.5 to 5.5 V		16	ns
			3.0 to 3.6 V		21	
			2.3 to 2.7 V		24	
			1.65 to 1.95 V		35	
Propagation Delay (E_{IN} to output E_{DET})	t_{pd_err}	C_L = 50 pF	4.5 to 5.5 V		11	ns
			3.0 to 3.6 V		13	
			2.3 to 2.7 V		15	
			1.65 to 1.95 V		25	
Input capacitance	C_{IN}	V_I = V_{CC} or GND	1.65 to 5.5 V	2	4	pF

Table 9: Dynamic characteristics

8. MODULE MECHANICAL DRAWING

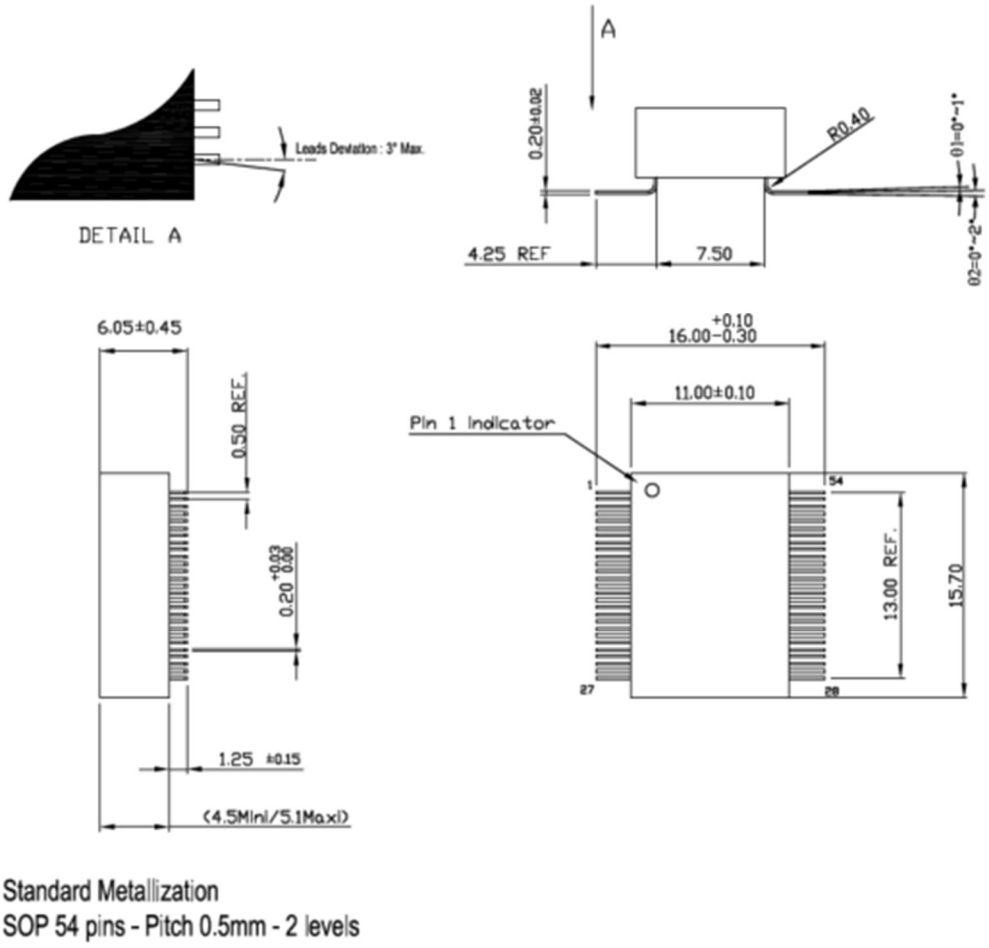

Figure 4 Mechanical drawing

9. PACKING, HNADLING, STORAGE AND MOUNTING REQUIREMENTS

9.1 PACKING

Modules are packed in boxes.

Each box is sealed with antistatic bag under vacuum with desiccant sachet.

Each packing is at least marked with:

- 3D PLUS Logo
- Module description: Octal 3-input Majority Voter
- Module P/N: See Table 2
- Quantity

9.2 HANDLING

3D PLUS modules must be handled with antistatic gloves and ESD wrist strap.

9.3 STORAGE

To avoid degradation due to humidity, components must be handled according to the following procedure:

- Storage in sealed bags: the calculated shelf life for dry sealed packed components is 12 months from the pack seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH. Beyond this period, the reconditioning is mandatory; modules shall be baked at 125°C during 48 hours.
- If the provided sealed bags are opened, please refer to 3D PLUS assembly recommendations (3300-1300/3300-8044)

9.4 BOARD ASSEMBLY

After sealed bag opening, 3D PLUS modules have to be baked 24 hours at 125°C. Caution: Device containers cannot be subjected to higher temperatures than their temperature limit indicated on the bag's label.

The use of any adhesive tape (e.g. Kapton®) on the side of the module during assembly is prohibited.

Module assembly on board must follow reflow guidelines as defined in: http://www.3d-plus.com/technical-documentation.php

The variants of the Octal 3-input Majority Voter module (see Table 2) are suitable for automatic and manual assembly process (3300-1300/3300-8044).

Module reinforcement, coating and leads tinning operation are also described in these documents.

Module cleaning after assembly must be done with isopropylic alcohol preferentially, or with de-ionized water otherwise. For other cleaning products, please consult 3D PLUS for further information.

9.5 ESD

To avoid ESD damage and to guarantee reliable assembling of the Octal 3-input Majority Voter module, 3D PLUS methods and instructions for ESD protections or equivalent have to be applied.

Human Body Model Classification (JS-001-2014) is 4000 V.

10. ORDERING INFORMATION

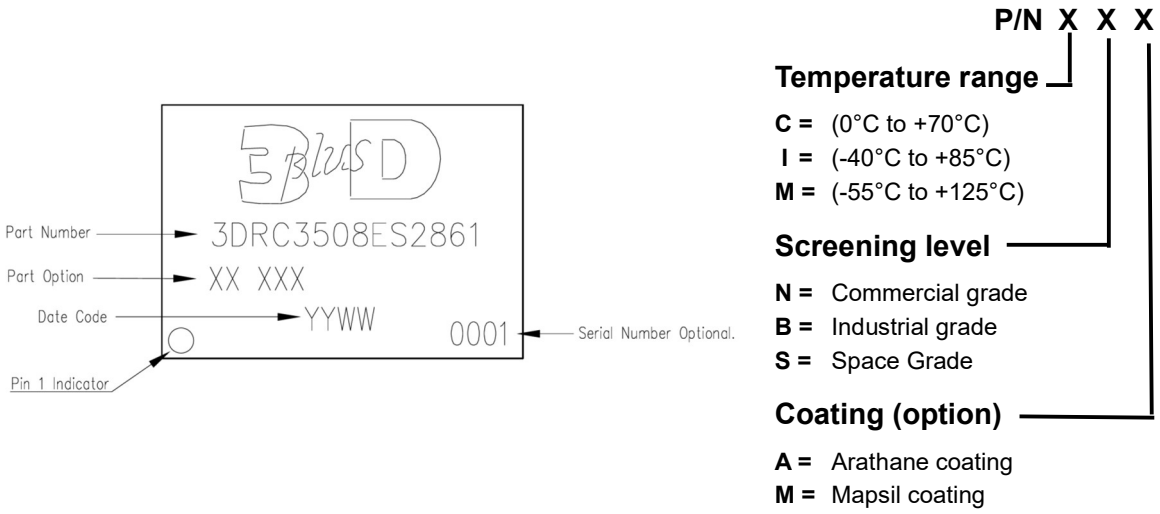

Figure 5 Ordering information.

11. REVISION HISTORY

ED./REV.	DATE (MM/DD/YYYY)	DESCRIPTION
1	12/19/2023	Initial document.
2	02/15/2023	Updated Table 6, removed $P_{CMAX,}$ notes added. Updated Table 8 I_{SB} and $I_{OFF.}$ Updated Table 9. Added section 9
3	09/19/2024	Updated Table 8 $I_{LIL,}$ I_{LIH} and $V_{OH.}$

Table 10: Revision history